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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,999	02/14/2002	Ken Takeuchi	001701.00140	9741

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BANNER & WITCOFF
1001 G STREET N W
SUITE 1100
WASHINGTON, DC 20001

EXAMINER	
HO, HOAI V	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,999	TAKEUCHI ET AL.	
	Examiner	Art Unit	
	Hoai V. Ho	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-60,62,63,65 and 66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-60,62,63,65 and 66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/667,610.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This office action is responsive to communication(s) filed on February 10, 2006.

2. Claims 47-60, 62, 63, 65 and 66 are presented for examination.

Claims 47, 48, 50, 55, 56 and 57 have been amended.

Claim Rejections - 35 USC 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 47, 48, 50, 55, 56 and 57 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. A newly added limitation "having a common node" in a "common latch circuit having a common node connected to one ends of said first and second bitlines" is not described in the specification. See figs. 9, 51 and 62.

5. Claim 57 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 57, line 8, "a third bit line connected to said second string line" is unclear and confusing. How does "second string line" in line 5 of claim 57 relate to "second string line" in line 7 of claim 57? Should "third" be changed to --second-- for clarifying? A phrase a "second bit line connected to said second string line" will be used for examination.

Claims 49, 51-54, 58-60, 62, 63, 65 and 66 are rejected due to the rejections of the parent claim.

Claim Rejections - 35 USC 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

The response has been reviewed but has not been found persuasive as to error in the rejections. Therefore, all claims that are still rejected for the same reason as set forth in the previous Office action are provided below for convenience including the rejections of newly added limitations such as string line replaces for memory cell section, a first or second select transistor connects to a first or second string line and having a common node to amended claims 47, 48, 50, 55, 56 and 57 as follows:

7. Claims 47-60, 62, 63, 65 and 66 are rejected under 35 U.S.C. 102(a) as being anticipated by Hemink et al. U.S. Pat. No. 5,870,334 (IDS).

Regarding to claims 47-50, 55-57 and 59, 60, 62, 63, 65 and 66, Figures 8 and 13 (col. 16, lines 17-20 and 28-31) of Hemink is directed to a nonvolatile semiconductor memory comprising: a first string line (a block of memory cells above a string of memory cells M1-M4 and a select transistor S2 connected to a main bit line BL in fig. 8, M4 in fig. 13 or M11 in fig. 20) including a first memory cell (such as M4 connects to select transistor) and a first select transistor connected in series (a select transistor connects between BL and the first memory cell above select transistor S2 in a lower block); a first bit line (a line connects between the first memory cell and the first switch) connected to said first string line; a second bit line (a line

connects between a second memory cell and a second switch); a second string line including a second memory cell (M4 in fig. 8) and a second select transistor (S2) connected in series [and said second bit line connected to said second string line]; a third bit line (not shown in fig. 8, however it has another same set of strings connects to BL); fourth bit line (not shown in fig. 8, however it has another same set of strings connects to BL); and a common latch circuit (103 of fig. 13 and col. 10, lines 26-38) having a common node (a connection at S2 and BL of fig. 13) connected to one ends (through the switch transistors S2) of said first, second, third and fourth bit lines, latching program / read data of at least one said first and third memory cells, wherein said first, second, third and fourth bit lines are different (by switch transistor S2) from each other; said first and second memory cells are programmed substantially simultaneously (controls by the same word line signal CG1, col. 14, lines 30, 31, 42 and 43), program data of said first memory cell is held by at least one of said first and second bit lines, and program data of said second memory cell is held by at least one of said third and fourth bit lines while a program voltage is supplied to said first and second memory (M2 or M21) cells (col. 10, line 24 to col. 11, line 20); a verify read operation to verify whether said first memory cell has been sufficiently programmed, is carried out by said common latch circuit, and program data of said third memory cell is held by said fourth bit line while conducting the verify read operation of said first memory cell; and said common latch circuit and said fourth bit line are electrically connected to each other, after the program data of said second memory cell held by said fourth bit line is transferred to said common latch circuit, a verify read operation to verify whether said second memory cell has been sufficiently programmed, is carried out using the program data of said second memory cell held by said common latch circuit, and while conducting a verify read operation of said

second memory cell, the program data of said first memory cell is held by said second bit line (col. 11, lines 21-24).

Regarding to claims 51-54, Figure 13 or 20 of Hemink discloses wherein said first memory cell (M1or M21) and said second memory cell (M2 of fig. 13 or M21 of fig. 20) are connected to different word lines (CG1 and CG2).

Regarding to claim 58, Figure 13 or 20 of Hemink discloses wherein said first (M1 of fig. 13 or M11 of fig. 20) and second memory (another memory cell connects in parallel with M1 or M12) cells are connected to a same word line (CG1).

8. Claims 47-60, 62, 63, 65 and 66 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakui et al. U. S. Patent No. 6307807 (PTO 892 see Mail Date 0404).

Figs 3 or 48 and 9 or 58, and 59 (for read, erase or writing) of Sakui are directed to a nonvolatile semiconductor memory comprising: a first string line (transistors connect to GSL, CGL and SSL signals of fig. 3 and 48) including a first memory cell (CGL) and a first select transistor (a select transistor SSL connects to BL0) connected in series; a second string line (an another section of transistors connect to GSL, CGL and SSL signals) including a second memory cell (CGL) and a second select transistor (a select transistor SSL connects to BL1) connected in series; a first bit line (BL0) connected to said first string line; a second bit line (BL1) connected to said second string line, being different from the first signal line; and a common latch circuit (20 of fig. 9 or fig. 58) having a common node (M1 connects to BLi) connected to one ends of said first and second bit lines; wherein first program/read data (figs. 48, 49 and 59) of said first memory cell (controlling by a signal SSL) is latched in said common latch circuit, while second program/read data of said second memory cell is held by said second bit line (controlling by a signal SSL).

Response to Arguments

9. Applicants' arguments have been fully considered but they are not persuasive.

Applicants argue that Hemink shows no separate bit line and bit lines are not connected to a common node of a common latch circuit. The Examiner disagrees with this statement, because Figs. 8 and 13 of Hemink show that each bit line (a line connects between the first memory cell and the first switch) of each string line is separated by the transistor switch S2 and connects to the common node (a connection at S2 and BL of fig. 13) of the common latch circuit (103 of fig. 13 and col. 10, lines 26-38). Figs 3 or 48 and 9 or 58 of Sakui show that each bit line (BLi) of each string line is separated by the transistor switch SSL and connects to the common node (M1 connects to BLi) of the common latch circuit (20 of fig. 9).

For the above reasons, it is believed that the rejections should be sustained. Feature of an invention not found in the claims can be given no patentable weight in distinguishing the claimed invention over the prior art.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai V. Ho whose telephone number is (571) 272-1777. The examiner can normally be reached on 7:00 AM -- 5:30 PM from Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

hvh
March 9, 2006

Hoai V. Ho
Primary Examiner
Art Unit 2827